

CLAIMS

1 1. (previously presented) A programmable device comprising a Serial Peripheral Interface
2 (SPI) adapted to be connected in parallel to an SPI interface of each of two or more SPI serial memory
3 devices such that the programmable device is adapted to receive a different portion of configuration data
4 stored in each SPI serial memory device without transmitting the configuration data via a controller
5 connected between the SPI serial memory devices and the programmable device.

1 2. (previously presented) The invention of claim 1, wherein:
2 the programmable device is an FPGA; and
3 each SPI serial memory device is an SPI serial flash PROM.

1 3. (previously presented) The invention of claim 1, wherein the programmable device is
2 adapted to independently generate at least one command adapted to control operations of each SPI serial
3 memory device during configuration of the programmable device.

1 4. (previously presented) The invention of claim 1, wherein the programmable device is
2 adapted to generate a message to inform each SPI serial memory device of a starting address to be used
3 to transfer the configuration data stored in said each SPI serial memory device to the programmable
4 device.

1 5. (previously presented) The invention of claim 1, wherein the programmable device is
2 adapted to receive instructions to ignore data from at least one of the SPI serial memory devices.

1 6. (original) The invention of claim 5, wherein the programmable device is adapted to
2 retrieve the instructions from the configuration data.

1 7. (canceled)

1 8. (previously presented) The invention of claim 1, wherein the programmable device is
2 adapted to be instructed, based on information contained in the configuration data, as to how to interpret
3 the different portions of the configuration data received from the different SPI serial memory devices.

1 9. (previously presented) The invention of claim 1, wherein the programmable device is
2 adapted to process different amounts of configuration data received from different SPI serial memory
3 devices.

1 10. (original) The invention of claim 9, wherein the two or more different SPI serial
2 memory devices are of two or more different sizes capable of storing the different amounts of the
3 configuration data.

1 11. (original) The invention of claim 9, wherein the programmable device is adapted to stop
2 including data from an SPI serial memory device that has already transmitted all of its configuration
3 data.

1 12. (previously presented) The invention of claim 1, wherein the programmable device
2 comprises:
3 a multiplexer (mux) adapted to interleave the configuration data from the two or more different
4 SPI serial memory devices; and

5 a timing controller adapted to control the operations of the mux and to generate a configuration
6 clock signal used to control the timing of the reading of the configuration data from the two or more
7 different SPI serial memory devices.

1 13. (original) The invention of claim 12, wherein the timing controller is adapted to (1)
2 change the operations of the mux and (2) change the rate of the configuration clock signal, when the
3 number of SPI serial memory devices having configuration data to transmit changes.

1 14. (previously presented) The invention of claim 1, wherein each different portion of the
2 configuration data from the corresponding SPI serial memory device is received at a different
3 configuration data input pin of the SPI interface of the programmable device.

1 15. (previously presented) The invention of claim 1, wherein each of one or more output
2 pins of the programmable device is adapted to be connected to corresponding pins of all of the SPI serial
3 memory devices.

1 16. (original) The invention of claim 15, wherein the programmable device has a
2 configuration clock signal pin adapted to be connected to corresponding configuration clock signal pins
3 of all of the SPI serial memory devices such that configuration data is transmitted simultaneously from
4 all of the SPI serial memory devices to the programmable device.

1 17. (previously presented) An apparatus comprising:
2 a programmable device having a Serial Peripheral Interface (SPI); and
3 two or more SPI serial memory devices, each having an SPI interface, wherein:
4 the SPI interface of the programmable device is connected in parallel to the SPI
5 interfaces of the SPI serial memory devices such that the programmable device is adapted to receive a
6 different portion of configuration data stored in each different SPI serial memory device without
7 transmitting the configuration data via a controller connected between the SPI serial memory devices and
8 the programmable device.

1 18. (previously presented) A method for configuring a programmable device, comprising:
2 reading a different portion of configuration data from a Serial Peripheral Interface (SPI) of each
3 of two or more different SPI serial memory devices connected in parallel to an SPI interface of the
4 programmable device without transmitting the configuration data via a controller connected between the
5 SPI serial memory devices and the programmable device; and
6 configuring the programmable device using the configuration data.

1 19. (currently amended) A programmable device adapted to be connected in parallel to two
2 or more memory devices such that the programmable device is adapted to receive configuration data
3 stored in the two or more memory devices without transmitting the configuration data via a controller
4 connected between any of the memory devices and the programmable device, wherein the programmable
5 device is adapted to receive a different portion of the configuration data from each different memory
6 device, and wherein one or more of (a)-(i):

7 (a) the programmable device has an SPI interface;
8 each memory device is an SPI serial memory device having an SPI interface; and
9 the SPI interface of each SPI serial memory device is connected to the SPI interface of
10 the programmable device;

11 (b) the programmable device is adapted to independently generate at least one command
12 adapted to control operations of the memory devices during configuration of the programmable device;

13 (c) the programmable device is adapted to generate a message to inform the memory
14 devices of a starting address to be used to transfer the configuration data stored in the memory devices to
15 the programmable device;

16 (d) the programmable device is adapted to receive instructions to ignore data from a
17 memory device;

18 (e) the programmable device is adapted to be instructed, based on information contained in
19 the configuration data, as to how to interpret the different portions of the configuration data received
20 from the different memory devices;

21 (f) the programmable device is adapted to process different amounts of configuration data
22 received from different memory devices;

23 (g) the programmable device comprises:
24 a multiplexer (mux) adapted to interleave the configuration data from the two or
25 more different memory devices; and

26 a timing controller adapted to control the operations of the mux and to generate a
27 configuration clock signal used to control the timing of the reading of the configuration data from the
28 two or more different memory devices;

29 (h) each different portion of the configuration data from the corresponding memory device
30 is received at a different configuration data input pin of the programmable device; and

31 (i) each of one or more output pins of the programmable device is adapted to be connected
32 to corresponding pins of all of the memory devices; and

33 the programmable device has a configuration clock signal pin adapted to be connected to
34 corresponding configuration clock signal pins of all of the memory devices such that configuration data
35 is transmitted simultaneously from all of the memory devices to the programmable device.

1 20. (original) The invention of claim 19, wherein:
2 the programmable device has an SPI interface;
3 each memory device is an SPI serial memory device having an SPI interface; and
4 the SPI interface of each SPI serial memory device is connected to the SPI interface of the
5 programmable device.

1 21. (currently amended) The invention of claim 19, wherein the programmable device is
2 adapted to independently generate the at least one command adapted to control the operations of the
3 memory devices during the configuration of the programmable device.

1 22. (currently amended) The invention of claim 19, wherein the programmable device is
2 adapted to generate [[a]] the message to inform the memory devices of [[a]] the starting address to be
3 used to transfer the configuration data stored in the memory devices to the programmable device.

1 23. (currently amended) The invention of claim 19, wherein the programmable device is
2 adapted to receive the instructions to ignore the data from [[a]] the memory device.

1 24. (original) The invention of claim 23, wherein the programmable device is adapted to
2 retrieve the instructions from the configuration data.

1 25. (currently amended) The invention of claim 19, wherein the programmable device is
2 adapted to be instructed, based on the information contained in the configuration data, as to how to
3 interpret the different portions of the configuration data received from the different memory devices.

1 26. (currently amended) The invention of claim 19, wherein the programmable device is
2 adapted to process the different amounts of configuration data received from the different memory
3 devices.

1 27. (original) The invention of claim 26, wherein the two or more different memory devices
2 are of two or more different sizes capable of storing the different amounts of the configuration data.

1 28. (original) The invention of claim 26, wherein the programmable device is adapted to
2 stop including data from a memory device that has already transmitted all of its configuration data.

1 29. (currently amended) The invention of claim 19, wherein the programmable device
2 comprises:

3 [[a]] the multiplexer (mux) adapted to interleave the configuration data from the two or more
4 different memory devices; and

5 [[a]] the timing controller adapted to control the operations of the mux and to generate [[a]] the
6 configuration clock signal used to control the timing of the reading of the configuration data from the
7 two or more different memory devices.

1 30. (original) The invention of claim 29, wherein the timing controller is adapted to (1)
2 change the operations of the mux and (2) change the rate of the configuration clock signal, when the
3 number of memory devices having configuration data to transmit changes.

1 31. (original) The invention of claim 19, wherein each different portion of the configuration
2 data from the corresponding memory device is received at a different configuration data input pin of the
3 programmable device.

1 32. (currently amended) The invention of claim 19, wherein each of one or more output pins
2 of the programmable device is adapted to be connected to corresponding pins of all of the memory
3 devices, wherein the programmable device has the configuration clock signal pin adapted to be
4 connected to the corresponding configuration clock signal pins of all of the memory devices such that the
5 configuration data is transmitted simultaneously from all of the memory devices to the programmable
6 device.

1 33. (canceled)

1 34. (currently amended) An apparatus comprising:
2 a programmable device; and
3 two or more memory devices, wherein:

4 the programmable device is connected in parallel to each memory device such that the
5 programmable device is adapted to receive configuration data stored in the two or more memory devices
6 without transmitting the configuration data via a controller connected between any of the memory
7 devices and the programmable device, wherein the programmable device is adapted to receive a different
8 portion of the configuration data from each different memory device, and wherein one or more of (a)-(i):

9 (a) the programmable device has an SPI interface;
10 each memory device is an SPI serial memory device having an SPI interface; and
11 the SPI interface of each SPI serial memory device is connected to the SPI interface of
12 the programmable device;

13 (b) the programmable device is adapted to independently generate at least one command
14 adapted to control operations of the memory devices during configuration of the programmable device;

15 (c) the programmable device is adapted to generate a message to inform the memory
16 devices of a starting address to be used to transfer the configuration data stored in the memory devices to
17 the programmable device;
18 (d) the programmable device is adapted to receive instructions to ignore data from a
19 memory device;
20 (e) the programmable device is adapted to be instructed, based on information contained in
21 the configuration data, as to how to interpret the different portions of the configuration data received
22 from the different memory devices;
23 (f) the programmable device is adapted to process different amounts of configuration data
24 received from different memory devices;
25 (g) the programmable device comprises:
26 a multiplexer (mux) adapted to interleave the configuration data from the two or
27 more different memory devices; and
28 a timing controller adapted to control the operations of the mux and to generate a
29 configuration clock signal used to control the timing of the reading of the configuration data from the
30 two or more different memory devices;
31 (h) each different portion of the configuration data from the corresponding memory device
32 is received at a different configuration data input pin of the programmable device; and
33 (i) each of one or more output pins of the programmable device is adapted to be connected
34 to corresponding pins of all of the memory devices; and
35 the programmable device has a configuration clock signal pin adapted to be connected to
36 corresponding configuration clock signal pins of all of the memory devices such that configuration data
37 is transmitted simultaneously from all of the memory devices to the programmable device.

1 35. (currently amended) A method for configuring a programmable device, comprising:
2 simultaneously reading configuration data from two or more memory devices connected in
3 parallel to the programmable device without transmitting the configuration data via a controller
4 connected between any of the memory devices and the programmable device, wherein the programmable
5 device receives a different portion of the configuration data from each different memory device; and
6 configuring the programmable device using the configuration data, wherein one or more of (a)-
7 (i):
8 (a) the programmable device has an SPI interface;
9 each memory device is an SPI serial memory device having an SPI interface; and
10 the SPI interface of each SPI serial memory device is connected to the SPI interface of
11 the programmable device;
12 (b) the programmable device is adapted to independently generate at least one command
13 adapted to control operations of the memory devices during configuration of the programmable device;
14 (c) the programmable device is adapted to generate a message to inform the memory
15 devices of a starting address to be used to transfer the configuration data stored in the memory devices to
16 the programmable device;
17 (d) the programmable device is adapted to receive instructions to ignore data from a
18 memory device;
19 (e) the programmable device is adapted to be instructed, based on information contained in
20 the configuration data, as to how to interpret the different portions of the configuration data received
21 from the different memory devices;
22 (f) the programmable device is adapted to process different amounts of configuration data
23 received from different memory devices;
24 (g) the programmable device comprises:
25 a multiplexer (mux) adapted to interleave the configuration data from the two or
26 more different memory devices; and

27 a timing controller adapted to control the operations of the mux and to generate a
28 configuration clock signal used to control the timing of the reading of the configuration data from the
29 two or more different memory devices;

30 (h) each different portion of the configuration data from the corresponding memory device
31 is received at a different configuration data input pin of the programmable device; and

32 (i) each of one or more output pins of the programmable device is adapted to be connected
33 to corresponding pins of all of the memory devices; and

34 the programmable device has a configuration clock signal pin adapted to be connected to
35 corresponding configuration clock signal pins of all of the memory devices such that configuration data
36 is transmitted simultaneously from all of the memory devices to the programmable device.

1 36. (previously presented) The invention of claim 1, wherein the different portions of the
2 configuration data are adapted to be simultaneously transmitted in parallel to the programmable device.

1 37. (previously presented) The invention of claim 17, wherein the different portions of the
2 configuration data are adapted to be simultaneously transmitted in parallel to the programmable device.

1 38. (previously presented) The invention of claim 18, wherein the different portions of the
2 configuration data are simultaneously transmitted in parallel to the programmable device.

1 39. (previously presented) The invention of claim 19, wherein the different portions of the
2 configuration data are adapted to be simultaneously transmitted in parallel to the programmable device.

1 40. (previously presented) The invention of claim 34, wherein the different portions of the
2 configuration data are adapted to be simultaneously transmitted in parallel to the programmable device.

1 41. (previously presented) A programmable device comprising a Serial Peripheral Interface
2 (SPI) adapted to be connected to an SPI interface of at least one SPI serial memory device such that the
3 programmable device is adapted to receive configuration data stored in the SPI serial memory device
4 without transmitting the configuration data via a controller connected between the SPI serial memory
5 device and the programmable device, wherein the programmable device is adapted to receive instructions
6 to ignore data from an SPI serial memory device.

1 42. (previously presented) The invention of claim 41, wherein the programmable device is
2 adapted to retrieve the instructions from the configuration data.